IN THE CLAIMS

Please amend the claims as follows. This claim set is to replace all prior versions.

1. (Currently amended) A power amplifier circuit for amplifying an input RF signal with respect to a specified RF output power, comprising

an input terminal for supplying the input RF signal to be amplified;

an output terminal for the RF signal with the output power specified;

an amplification path formed between the input terminal and the output terminal having a power amplification circuit for amplifying the RF signal;

a bypass formed between the input terminal and the output terminal for the RF signal to bypass the amplification path;

a control terminal for controlling the operation of the amplification path and the bypass, such that an RF signal is either passed through the amplification path or the bypass;

a variable gain amplifier circuit for pre-amplification of the input RF signal which is placed between the line from the input terminal to the amplification path and the bypass; and

a delay control means for controlling the variable gain amplifier, the amplification path, and the bypass[[;]], such that when the RF output power of the RF signal is to be increased, a variable gain of the variable gain amplifier circuit is reduced before operating conditions of the amplification path and the bypass are set, after a delay time period, to a state in which the RF signal is passed through the amplification path to achieve the output power specified, and vice versa when the RF output power of the RF signal is to be reduced.

~~wherein the variable gain amplifier, the amplification path, and the bypass in a first state are operable to achieve the RF output power specified, and wherein the delay control means is operable to configure the variable gain amplifier, the amplification path, and the bypass in a second state that is an inverse of the first state.~~

2. (Currently amended) A power amplifier circuit according to claim 1, wherein the ~~a~~ delay time period ~~for which the delay control means configures the variable gain amplifier,~~

~~the amplification path, and the bypass in the second state~~ corresponds to half a settling time (τ) for an RF output power change.

3. (Previously Presented) A power amplifier circuit according to claim 1, wherein the delay control means comprises:
a latch trigger circuit for controlling the operation of the amplification path and the bypass;
a sample-and-hold circuit for controlling the gain factor of the variable gain amplifier circuit;
a digital multiplexer circuit for selecting a control signal; and
a delay circuit for delaying a control signal by a delay time period.

4. (Previously Presented) A power amplifier circuit according to claim 1, wherein the bypass comprises:
a first matching circuit;
a second matching circuit; and
a first controllable switch for configuring an impedance of the bypass to control passage of the RF signal.

5. (Previously Presented) A power amplifier circuit according to claim 1, wherein the amplification path comprises:
a third matching circuit; and
a controllable second switch for adjusting an impedance of the amplification path to either amplify the RF signal or block the passage of the RF signal.

6. (Previously Presented) A power amplifier circuit according to claim 1, wherein the control terminal is configured to provide control information to the delay control means.

7. (Previously Presented) A power amplifier circuit according to claim 1, wherein the variable gain amplifier circuit comprises a digital and/or analogue gain control.

8. (Previously Presented) A power amplifier circuit according to claim 1, wherein the input RF signal is a signal coded for use in an UMTS communication system.

9. (Previously Presented) A mobile terminal for a wireless telecommunication system comprising a power amplifier circuit ~~(1")~~ according to claim 1.

10. (Currently amended) A method for amplifying an input RF signal with respect to a specified RF output power, comprising:

supplying the input RF signal to be amplified;

outputting the RF signal with the output power specified;

amplifying the RF signal in an amplification path formed between an input terminal and an output terminal;

selectively bypassing the amplification path using a bypass;

controlling operation of the amplification path and the bypass such that an RF signal is either passed through the amplification path or the bypass;

pre-amplifying the input RF signal by a variable gain amplifier circuit which is placed between the line from the input terminal to the amplification path and the bypass ; and

controlling the variable gain amplifier the amplification path, and the bypass by a delay control means[[;]], such that when the RF output power of the RF signal is to be increased, a variable gain of the variable gain amplifier circuit is reduced before operating conditions of the amplification path and the bypass are set, after a delay time period, to a state in which the RF signal is passed through the amplification path to achieve the output power specified, and vice versa when the RF output power of the RF signal is to be reduced.

~~operating the delay control means to configure the variable gain amplifier, the amplification path, and the bypass in a first state that is an inverse of a second state; then~~

~~operating the variable gain amplifier, the amplification path, and the bypass in the second state to achieve the RF output power specified.~~

11. (Currently amended) A method according to claim 10, wherein the ~~a~~ delay time period ~~for which the delay control means configures the variable gain amplifier, the~~

~~amplification path, and the bypass in the first state~~ corresponds to half a settling time (τ) for an RF output power change.

12. (Previously Presented) A method according to claim 10, wherein operating the delay control means comprises:
controlling operation of the amplification path and the bypass by a latch trigger circuit integrated in the control means;
controlling the gain factor of the variable gain amplifier circuit by a sample-and-hold circuit
selecting a control signal by a digital multiplexer circuit; and
delaying a control signal by a delay time period by a delay circuit.

13. (Previously Presented) A method according to claim 10, wherein selectively bypassing the amplification path comprises:
adjusting an impedance of the bypass to control passage of an RF signal using a first matching circuit, a second matching circuit, and a first controllable switch integrated in the bypass.

14. (Previously Presented) A method according to claim 10, wherein amplifying the RF signal comprises:
adjusting an impedance of the amplification path to either amplify an RF signal or block the passage of the RF signal using a third matching circuit and a controllable second switch integrated in the amplification path.

15. (Previously Presented) A method according to claim 10, wherein controlling operation of the amplification path comprises:
configuring a control terminal to provide control information to the delay control means.